Quantum Cost Efficient Design of 4 Bit Johnson Counter Using Reversible Gate

Anirban Dutta, Heranmoy Maity, Arindam Biswas, Anup Kr. Bhattacharjee and Anita Pal

Abstract

Over the last few decade reversible logic circuits have attracted considerable attention in improving some fields like nanotechnology, quantum computing, cryptography, optical computing and low power design of circuits due to its low power dissipating characteristic. Research is going on in the field of reversible logic and a good amount of research work has been carried out in the area of reversible combinational logic. However, there is not much work in the area of sequential circuit like flip-flops and counters. In this paper we proposed the design quantum cost efficient of 4-bit Johnson counter with reduced number of quantum cost and constant inputs using existing reversible logic gate. The proposed work is design using two type of D flip-flops, one D flip-flop is design using SAM gate and Feynman gate with Q output only, others D flip-flop is design by SAM gate and Double Feynman gate with both Q and Q' outputs terminals. The proposed work is derived with quantum cost, constant inputs, garbage output and number of gates.

Keywords

Quantum computing, Reversible logic, Johnson counter, Quantum cost, Garbage output

I. Introduction

The 4-bit Johnson counter can be design using 4 D flip-flop. In this paper we proposed the quantum cost efficient 4-bit reversible Johnson counter with reduced number of quantum cost and constant inputs using existing reversible logic gate. This paper organized as follow: Section-2 describes the basic concepts of reversible logic, Section-3 describes the proposed work, Section-4 describes the analysis and discussion of the proposed work and section-5 conclusion.

II. Basic Concepts

A. Reversible Logic Gate

It is a P×P logic function in which P is the number of inputs and number of outputs. Inputs and outputs are one-to-one correspondence, i.e. outputs can be uniquely determined from the inputs and also the inputs can be recovered from the outputs [1-5]. The garbage output(GO) refers to the number of unused outputs present in the reversible logic circuits. Quantum cost(QC) refers to the cost of the circuit in terms of the cost of a primitive gate. The quantum cost of a reversible gate is the number of 1x1 and 2x2 reversible gates or quantum gates required in its design. The quantum costs of all reversible 1x1 and 2x2 gates are taken as unity [3]. The delay of a logic circuit is the maximum number of gates in a path from any input line to any output line. There are several reversible logic gates, but in this paper we use only 3×3 SAM gate with QC 4[4], 2×2 Feynman gate(FG)[3] with QC 1and 3×3 double Feynman gates(DFG) with 2 QC[5] is used. Fig. 1 and Fig. 2 shows the block diagram and quantum representation of SAM gate. Fig. 3 and Fig. 4 shows the block diagram and quantum representation of Feynman gate and Fig. 5 and Fig. 6 shows the block diagram and quantum representation of DFG.

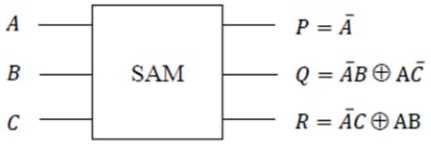

Fig.1. *Block diagram of SAM gate*

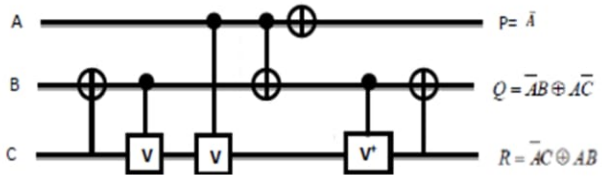

Fig. 2. *Quantum representation of SAM gate.*

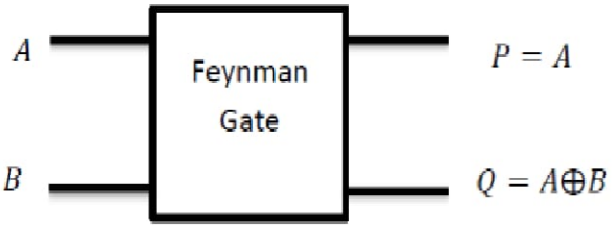

Fig. 3. *Block diagram of Feynman gate.*

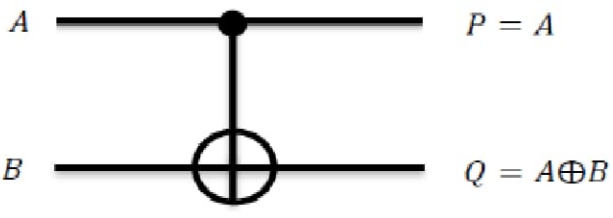

Fig 4. *Quantum representation of Feynman gate.*

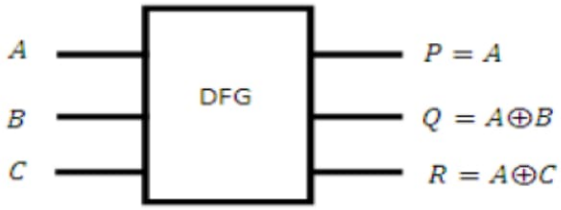

Fig. 5. *Block diagram of DF gate*

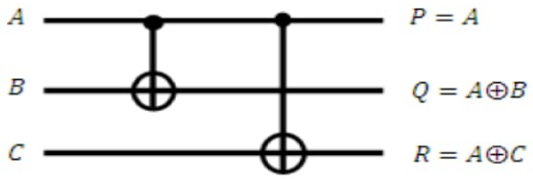

Fig 6. *Quantum representation of DF gate.*

B. D Flip-flip

The Fig. 7 and Fig. 8 shows the block diagram of D Flip-flop[4,6]. In Fig.7 D Flip-flop has only one Q output terminal with quantum cost 5 and in Fig. 8 D Flip-flop has two output terminal Q and Q' with quantum cost 6.

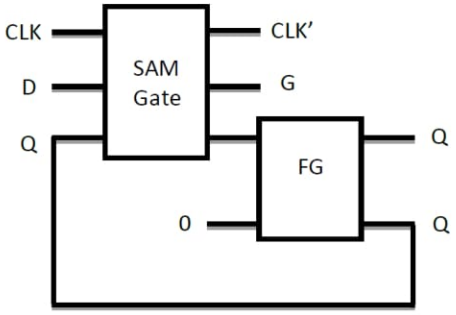

Fig 7. *Block diagram of D Flip-flop with Q output.*

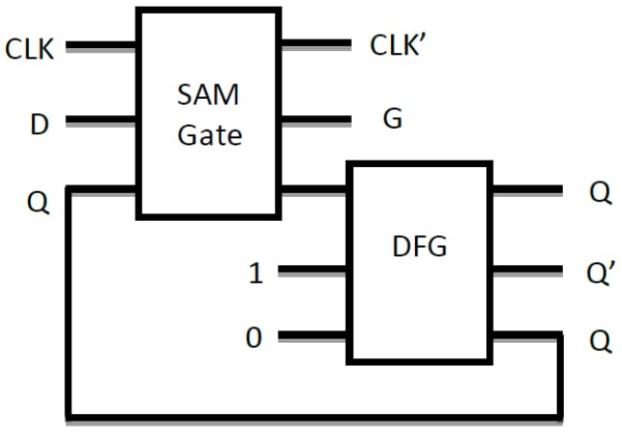

Fig. 8. *Block diagram of D Flip-flop with Q and Q' outputs.*

III. Proposed Quantum Cost Efficient Johnson Counter

The Johnson counter is constructed by connecting the inverted output of the last flip-flop to the input of the first flip-flop. The truth table given in Table-1, one can observe that, for a 4-bit Johnson counter, there are 8-states.

Table 1. Truth table of 4-bit Johnson Counter

CLK	Q1	Q2	Q3	Q4
0	0	0	0	0
1	1	0	0	0
1	1	1	0	0
1	1	1	1	0
1	1	1	1	1
1	0	1	1	1
1	0	0	1	1
1	0	0	0	1
1	0	0	0	0

The Fig. 9 shows the proposed design of Johnson counter using SAM gate, Feynman gate and Double feynman gate. CLK is the clock input terminal and Q1, Q2, Q3 and Q4 are the outputs terminal of Johnson counter. G1, G2, G3 and G4 are the garbage output terminals.

IV. Analysis and Discussion

In the implementation of 4-bit Johnson counter we use four SAM gate having Quantum cost(QC) of 4×4=16, three feynman gate(FG) having Quantum cost =1×3=3 and one double Feynman gate(DFG) having 2×1=2 quantum cost. Total quantum cost required to design proposed Johnson counter is 21. Number of gates quantum cost, constant inputs, garbage output are shown in Table-2.

Table. 2

	No of Gates	Quantum Cost	No. of constant input	No. of garbage output
Proposed Design	8	21	5	4
Existing[7]	8	24	8	4

V. Conclusion

We have presented the basic concepts of reversible logic gates. Such gates can be used in regular circuits realizing Boolean functions. This paper proposes designs of quantum cost efficient Johnson counter using existing reversible logic gate. Here in this paper the proposed designs are better in terms of quantum cost, number of constant inputs and garbage outputs. The proposed design can have great impact in quantum computing. The proposed design has the applications in nanotechnology, low power circuit design, cryptography, optical computing etc.

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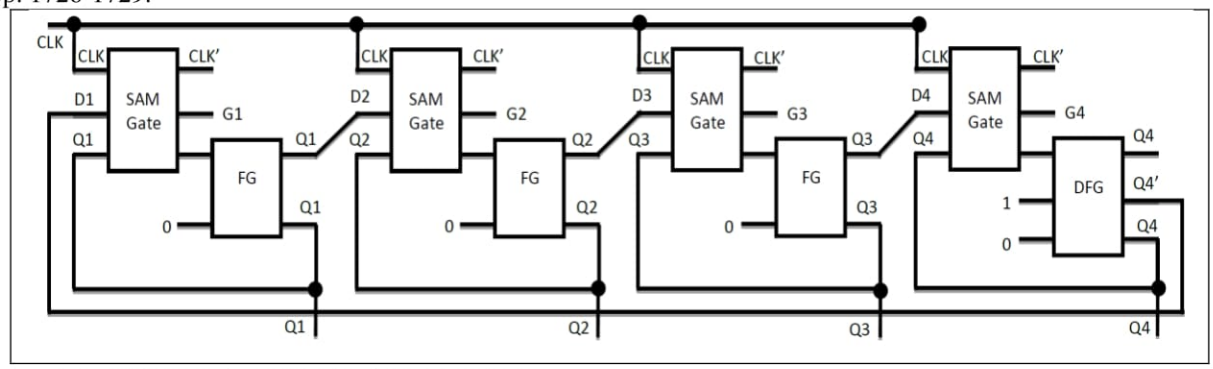

Fig. 9 Proposed Design of Johnson Counter.

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