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Implementation of 1 bit CMOS Full Adder Design and Analysis Based on Propagation Delay

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Abstract

This paper presents a high speed 1-bit CMOS Full Adder design and analysis based on propagation delay using 250nm technology. The transistor sizes are optimized precisely for low propagation delay without affecting the basic operation of full adder with a supply voltage of 5V. There are three important factors in CMOS: i.e. the transistor size area, power dissipation and speed of operation which always compromise between them when it is implemented in the field of IC circuit design. This paper proposes high speed design of full adder in compared to the existing conventional adder in terms of its propagation delay with the schematic and simulation results in Tanner tool version 16.

Keywords: *XOR, Full Adder, CMOS logic, VLSI, Propagation Delay, Transistor count.*

I. Introduction

Addition is one of the fundamental arithmetic operations and is used extensively in many VLSI system[2] such as application-specific DSP architectures and microprocessor and often one of the speed-limiting elements. Adder is the core element of complex arithmetic circuits like addition, multiplication, subtraction, division, exponentiation address calculation and generation in case of cache memory etc. The XOR-XNOR circuits are basic building blocks in various circuits[9] especially Arithmetic circuits, Compressors, Comparators, Parity Checkers, Code Convertors, Error detecting and correcting codes and Phase Detector.

There are several implementations with various logic styles that have been used in the past to design full adder cells. The logic style used in gates basically influences the speed, size, power dissipation and the wiring complexity of a circuit. The circuit delay is determined by number of inversion levels, the number of transistor[12][6] in series, transistor sizes (i.e. channel width) and intra-cell wiring capacitances. Transistor sizes (widths) determines (i) Speed[10] of circuit (ii) Energy consumption (iii) Total area of circuit (iv) Satisfaction of delay constraints. Hence optimization of the adder both in terms of speed and/or power consumption[13] should be pursued.

In these paper we present two different 1 bit CMOS full adder circuits with suitable propagation delay performance[8]. We have simulated two full adder circuits, one is conventional and other is proposed full adder circuit and compared[4] the propagation delay of the proposed full adder cell with the conventional full adder circuit. The remainder of the paper is organised as follows. In section II discusses all the CMOS 1-bit full adder circuits used for comparison[3]. Section III provides the simulation results (delay and transistor count) of all the circuits shown in section II. Section IV ends up with the conclusion.

II. Complementary CMOS logic style

Different logic styles tend to favour one performance aspect at the expense of others. In the other words, it is different design constraints[1] imposed by the application that each logic style has its place in the cell library development. Even a selected style appropriate for a specific function may not be suitable for another one.

In recent years several variants of different logic styles have been proposed to implement 1-bit adder cells. These papers have also investigated different approaches[5] realizing adders using CMOS technology; each has its own pmos and nmos. Scaling the supply voltage appears to be most well-known means to reduce power consumption. However lowering supply voltage[14] increases circuit delay and degrades the drivability of cells designed with certain logic style. One of the most important obstacles in decreasing supply voltage is the large transistor count and Vth loss problem. The advantages of complementary CMOS logic circuit are its layout regularity and stability at low voltage due to the complementary transistor pairs and smaller number of interconnecting wires.

A.Conventional CMOS logic style: A basic cell in digital computing systems is the 1-bit full adder which has 1-bit inputs (A, B and C) and two 1-bit outputs (Sum and Carry).The addition of two bits (A and B) with input carry C generates the sum bit and the output carry bit. The relations between the input and outputs are expressed as: Sum= A^B^C = ABC+Carry'(A+B+C).Carry= AB+BC+CA = AB+(A+B)C. The Complementary CMOS full adder has 28 transistors and is based on the regular CMOS structure (pull-up and pull-down networks). The conventional complementary CMOS full adder schematic is shown in Fig. 1. And the transient response/simulated output waveform is also shown in Fig. 2.

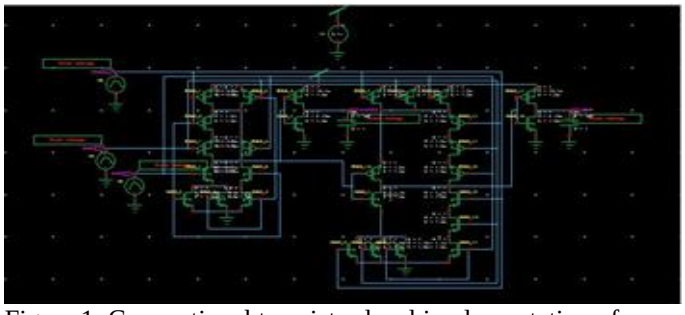

Figure 1: Conventional transistor level implementation of CMOS 1-bit full adder

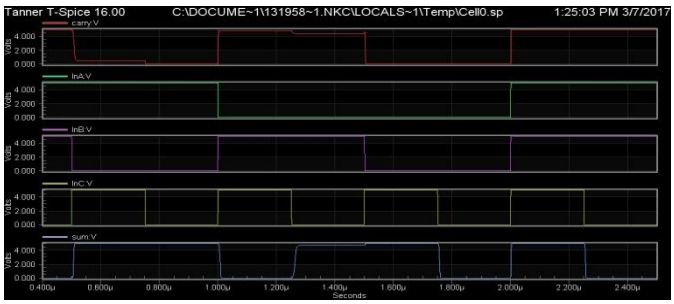

Figure 2: Transient response or output voltage waveform of conventional full adder(Vdd=5v)

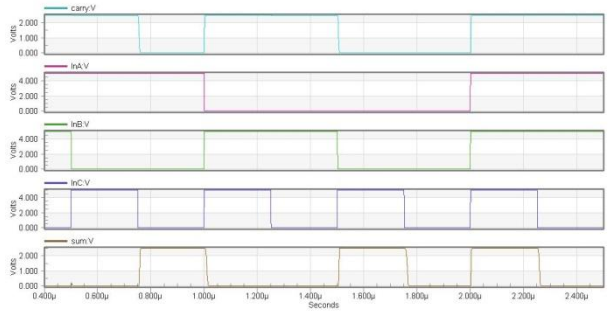

Figure3:Transient response/output voltage waveform of conventional full adder (Vdd=2.5v)

B.Proposed CMOS logic style: The desig of proposed CMOS full adder is based on 30 ransistors composed of two XOR[11] gates and three NAND gates. It shows the better performance than the earlier designed full adder and acquires less silicon area as the aspect ratio of transistors are less compared to the previous one.The Boolean equations for the design of proposed full adder are as follows:

Sum=A^B^C=(A^B)C'+(A^B)'C=((AB+A'B')')C'+(AB+A'B')C ; Carry=AB+(A^B)C

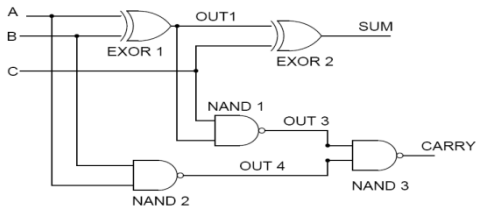

Figure 4:Block diagram of proposed CMOS 1-bit full adder

However, the improvement in speed over conventional CMOS adder is eminent and drastically leads to a better power-delay product[7]. The transistor-level implementation of proposed CMOS full adder schematic is shown in Fig3 below.

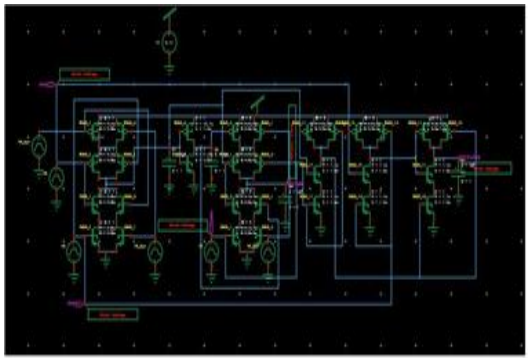

Figure 5: Proposed transistor level implementation of CMOS 1-bit full adder

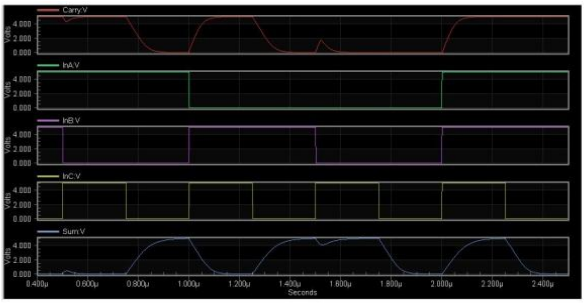

Figure 6:Transient response/output voltage waveform of conventional full adder (Vdd=5v)

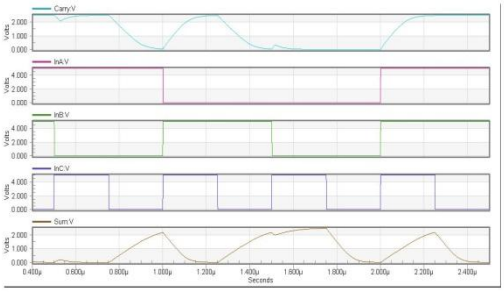

Figure 7: Transient response/output voltage waveform of conventional full adder (Vdd=2.5v)

Table:1 Specification of MOSFETs in different logic gates

SL.NO	EXOR1	EXOR2	NAND1	NAND2	NAND3	INV
IN1	A	OUT 1	OUT1	A	OUT 3	OUT1
IN2	B	C	C	B	OUT 4	
OUT	(A^B) = OUT1	A^B^C = SUM	~((A^B) C) = OUT3	~(A.B) = OUT4	CARRY	~OUT1 = OUT2
Wp	800n	200n	200n	200n	200n	15.7u
Wn	200n	100n	100n	100n	100n	2.15u
Lp	0.5u	0.5u	0.5u	0.5u	0.5u	0.5u
Ln	0.5u	0.5u	0.5u	0.5u	0.5u	0.5u

III.Simulation Results and Discussions:

This section presents simulation setup and results. Complementary conventional and proposed CMOS full adder

considered in this work are simulated for estimation of propagation delay and its comparative results are reported in this section.

We have performed simulations using Tanner EDA tool in 250nm technologies; with supply voltage ranges from 2.5v to 5v. To establish an impartial testing environment each circuit have been tested on the same input patterns. The input test pattern we have used consists of the three input signals A, B, and C and these signals are square waves of equal on and off times.

A.Specification of elements for input test pattern:

Table:2 Specification of input elements

Elements (input)	Pulse Width	Pulse Period	Voltage levels
A	**1us**	**2us**	**Vh=5v; Vl=0v**
B	**500ns**	**1us**	**Vh=5v; Vl=0v**
C	**250ns**	**500ns**	**Vh=5v; Vl=0v**
capacitor	**-**	**-**	**C=1pF**

Each one-bit full adder has been analysed in terms of propagation delay. For each transition, the delay is measured from 50% of the input voltage swing to 50% of the output swing.The maximum delay is taken as the cell delay. It is apparent from Fig that in this paper the proposed adder cell has smallest delay than conventional adder.

B.Transient Analysis set-up:
Start time =400ns ; stop time =1000ns ; maximum time step=1us; print start time=400ns.

C.Propagation Delay comparison: All transistors are having the same specifications and the transient response of each design is taken, keeping the three input pattern as well as the simulation set-up for transient analysis same.

Table:3 Propagation delay comparison in different CMOS logic design style

CMOS Design style	Sum output	Carry output
Conventional	t_{PHL}=143.92ns t_{PLH} =21.86ns	t_{PHL}= 58.12ns t_{PLH} =166.27ns
Proposed	t_{PHL}= 22.68ns t_{PLH} =7.4ns	t_{PHL}=19.55ns t_{PLH}=142.56ns

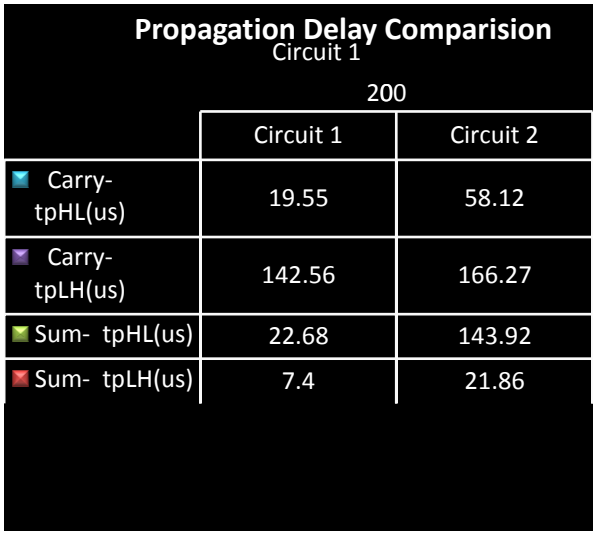

Figure 8:Comparison chart of two different CMOS full adder in terms of propagation delay

IV. CONCLUSION

In this paper two different 1-bit CMOS full adder logic design styles have been implemented, simulated, analysed and compared. This together with its significant delay reduction makes it the circuit of choice for low-power, low-voltage and high performance implementation, like multipliers. we have designed an advanced or faster CMOS 1-bit full adder using 250nm technology having minimum number of transistors and low propagation delay. It gives us the advantages of less complexity in designing the circuit and less propagation delay in compared to the conventional results i.e, initially for sum output t_{PHL}=143.92ns t_{PLH} =21.86ns and for carry output t_{PHL}=58.12ns t_{PLH} =166.27ns for 28 transistors. Performance has been improved after using proposed full adder where the values of propagation delay are reduced to for sum output t_{PHL}=22.68ns t_{PLH} =7.4ns and for carry output t_{PHL}=19.55ns t_{PLH} =142.56ns.

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